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Low Power Dynamic Logic Ripple Carry Adder Using Footed Diode Domino Logic

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ABSTRACT
In recent electronic devices power saving has more importance than any other thing. Dynamic logic circuits are one of the basic power efficient circuits which comes into picture when dealt with low power. Dynamic logic circuits operate mainly in two phases, namely Pre-charge and evaluate phase. Domino logic circuits are more power efficient and cooperatively faster circuits which operate on the above two phases. For extremely low power applications footed diode domino logic is applied. This paper mainly deals with design of Dynamic logic circuit design based on footed diode domino logic with reduction in power and leakage current. In this proposed circuit we put a diode on the foot of domino logic circuit which results in power reduction as compared to reported and conventional domino logic. We are using NMOS as a diode and due to this extra diode (NMOS), in pre-charge period leakage current reduce due to stacking effect. Approximately 32% of power is saved using footed diode domino logic.
For Simulation we are using tanner tool at 180nm technology.
Keywords: Fulladder, Footed diode domino logic, Pseudo dynamic logic, Ripple carry adder, Stacking effect

I. INTRODUCTION

Low power and high speed logic design circuits continue to get more attention in consideration of product manufacturing. So now a day's power saving has more importance than any other thing. Dynamic logic circuits came into the picture because of power efficient circuitry. Domino logic circuits are more power efficient and cooperatively faster, so these circuits have almost half the transistor count with respect to complementary static circuits. Domino logic is basically a dynamic logic circuit followed by a static inverter and having a capacitor as a load. The clock signal is used to control the operation of domino logic circuit . The output of the dynamic logic circuit is stored in the parasitic capacitance which is located just before the static inverter .

The parasitic capacitance just stores the output voltage and passes it to the next state which is the output stage of the domino circuit and stored in the load capacitor . The dynamic logic circuit requires two phases. The first phase, when Clock is low, is called the pre-charge phase and the second phase, when Clock is high, is called the evaluation phase . In the setup phase, the output is driven high unconditionally (no matter the values of the inputs). The capacitor, which represents the load capacitance, becomes charged. Because the transistor at the bottom is turned off, it is impossible for the output to be driven low during this phase. During the evaluation phase, Clock is high. In the pre-charge

phase also extra noise is introduced to the dynamic circuit .

II. PREVIOUS MODELS
2.1 Conventional Domino Logic

The schematic of a conventional footed clock controlled domino logic circuit, which consists of a dynamic N-type gate (Pull-down network PDN) followed by a static inverter. Fig 1. illustrates the implementation of a domino logic buffer. The gate operates in two phases, namely pre-charge and evaluation phases. During the pre-charge phase the clock signal clk is pulled low thus turning on the PMOS transistor M1 enabling to pre-charge the dynamic node Z. During the evaluation phase , the clock signal clk is pulsed high ,thus turning on the NMOS transistor M2. When the input A is low ,the logic at node Z is kept high regardless of the operating phase .However, when the input A is high ,two phases(evaluation and pre-charge)should be discussed as depicted in Fig 2 .

During the pre-charge phase, node Z is charged up to V_{dd} as well as node B. The voltage at node F drops downto'0', resulting in a propagation of the pre-charge phase to the output of the buffer. The propagation of the pre-charge pulse from node Z through the static buffer results in increased power consumption .In addition, the output logic is unstable during the pre-charge phase.

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logic is unstable during the pre-charge phase and as a

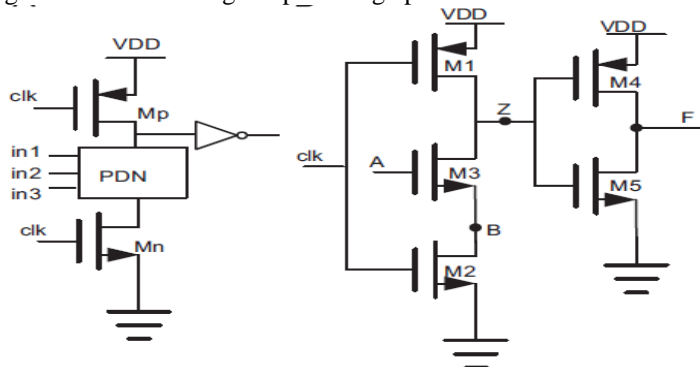result the cascading performance is limited
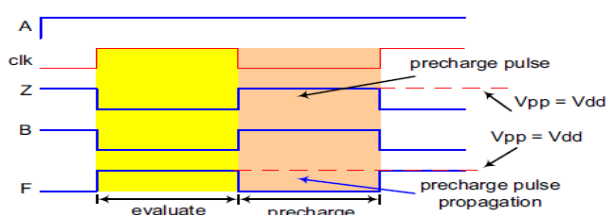

Fig1: Conventional domino logic

Fig 2 : Timing diagram of conventional domino logic

2.2 Pseudo Based Domino Logic

The previous section illustrates the issue of performance degradation due to the propagation of the pre-charge pulse inherent in domino logic gates .The proposed PDB-based implementation over comes this problem using the circuit structure shown in Fig 3.In the proposed implementation of the buffer,the source of the buffer's NMOS transistor M5 is connected to node B instead of Gnd. Using such a circuit topology ,the value at node Z cannot propagate to the output F during the pre-charge phase of the gate since during this phase, the evaluation transistor M2 is turned off .For our proposed gate, when the input logic A is low, the floating node Z is always high and then, the output node F is kept low regardless of the operating phase .On the other hand ,if the input A is high ,the pre-charge and evaluation phases will lead to the following situation.

During the evaluation phase,node Z is discharged to G_{nd} as well as node B, resulting in enabling the PMOS transistor M4, while pulling up the output F to V_{dd}.

During the pre-charge phase node Z is charged up to Vdd , followed by the voltage at node B. Since the NMOS evaluation transistor M2 is disabled the output node Z is held high. It is important to note that during the pre-charge phase ,the output node F is isolated from Gnd. In other words the pre-charge pulse at node Z cannot propagate through the buffer to the output node F.
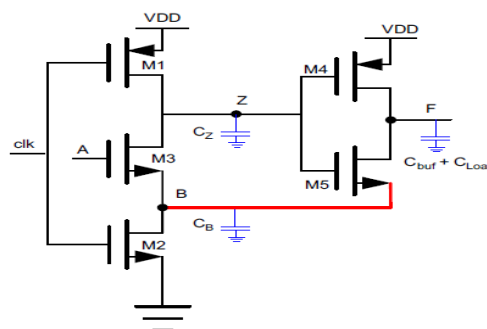

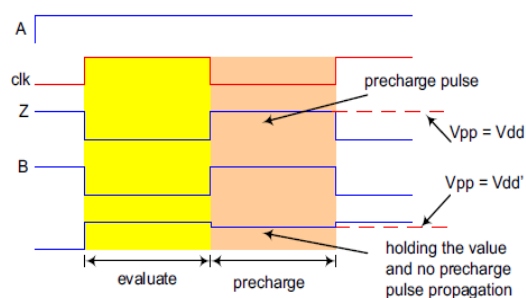Fig 3: Domino logic circuit using the proposed pseudo dynamic buffer.

Fig 4: Timing diagram of pseudo based domino logic

2.3 Footed Diode Domino Logic

Performance degraded in a circuit is due to propagation of pre-charge pulse from dynamic node to the output node. The PDB based design for domino logic compensates this problem up to some extent but there is always a room for improvement. In our proposed circuit we put an NMOS transistor which is working as a diode in between GND and M2

clock transistor. Let us take an example of a diode footed buffer shown in the fig 5. In the circuit shown in the fig.5. the source of the NMOS transistor m5 is connected to the node B instead of the GND. An NMOS transistor is introduced in the circuit whose gate is shorted with its drain and connected to the source of the NMOS clock transistor M2, the source of NMOS transistor M6 is connected to ground. In the circuit when input A is low then dynamic node Z is always high and output is kept low regardless of operating phase.
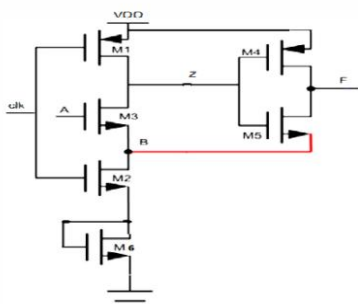

Fig 5*:* Footed diode domino logic

III. DESIGNED CIRCUITS
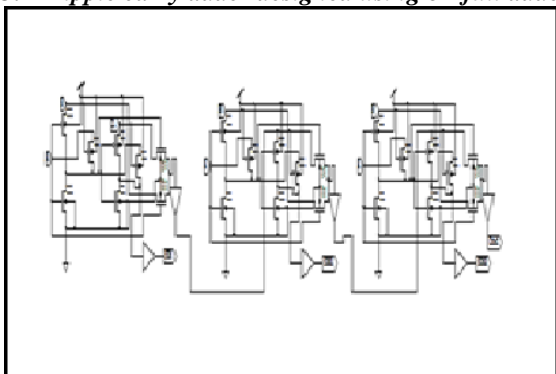### 3.1 *Ripple carry adder designed using 8T full adder*

Fig 6**:** Ripple carry adder
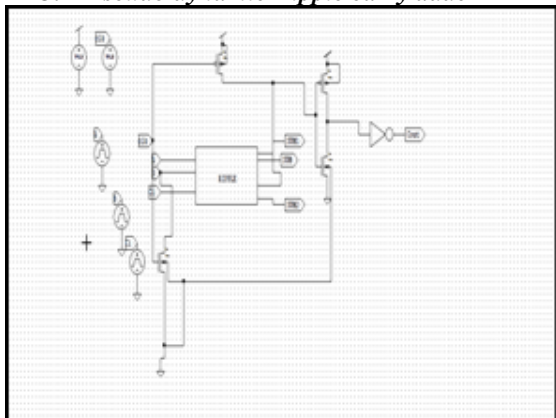
3.2 *Pseudo dynamic Ripple carry adder*

Fig7**:** Pseudo dynamic ripple carry adder circuit

Here the source of one NMOS transistor is connected to drain of another NMOS transistor.
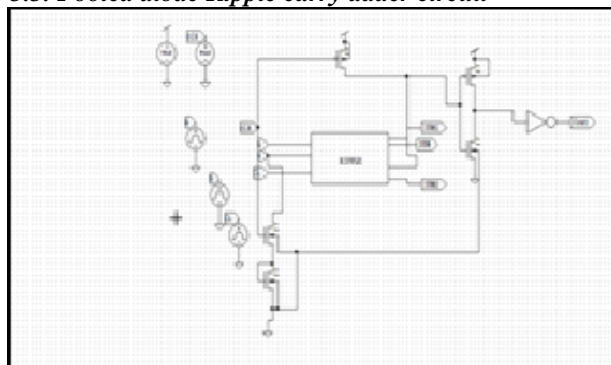
3.3. *Footed diode Ripple carry adder circuit*

Fig 8: Footed diode Ripple carry adder

IV. SIMULATION RESULTS
The below figure shows the simulation results of Ripple carry adder circuit
- Given inputs are for A-000,B-111,Ci-1
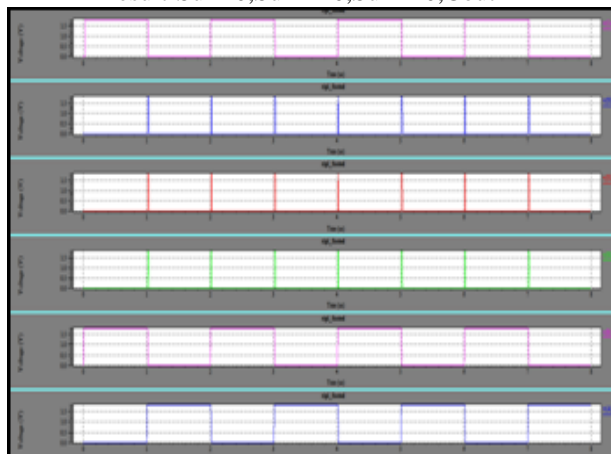- Result-Sum-0,Sum1 -0,Sum2-0,Cout-1

Fig 9: Simulated results

V. P0WER RESULTS TABLE

Pseudo dynamic ripple carry adder	6.667595e-005 watts
Footed diode ripple carry adder	5.253873e-005 watts

Table1: Power results of ripple carry adder

In particular serially connected devices or stacked devices have lower leakage than the sum of the leakages of all devices consumed individually. An informal definition of stack effect is: the total leakage current of cascaded transistor chain decreases with the number of stacked transistors increasing, and it is often used to reduce leakage power

Stack effect is not only a phenomenon of transistors, but also that of whole circuits. The sub

threshold leakage current flowing through a stack of transistors connected in series, is reduced if at least one of them is switched *off*.

To demonstrate the stack effect of transistors we have to conduct experiments to calculate the total leakage currents for different number of cascaded PMOS and NMOS transistors with high and low threshold voltages

VI. CONCLUSION

Due to propagation of the pre-charge pulse to the output node in conventional domino logic increased the power dissipation by the circuit. The propagation of pre-charge pulse to output node is prevented by using pseudo domino logic and some power has been saved. This paper proposes a footed diode domino logic style design which can reduce leakage current and more power has been saved as compared to other logic style. Approximately 32% of power is saved using footed diode domino logic compared to pseudo domino logic.

REFERENCES

[I]   M. Anders, S. Mathew, B. Bloechel, S. Thompson, R. Krishnamurthy,K. Soumyanath, S. Borkar, A 6.5 GHz 130 nm single-ended dynamic ALU and instruction-scheduler loop, IEEE ISSCC (2002), pp. 410-411.

[2]   Xu-guang Sun, Zhi-gang Mao, Feng-chang Lai, A 64 bit parallel CMOS adder for high performance processors, in: Proceedings of the IEEE ASia-Pacific Conference on ASIC, 2002, pp. 205-208.

[3]   R.H. Krambeck, C. M. Lee, H.-F.S. Law, High-speed compact circuits with CMOS,IEEE Journal of Solid-State Circuits, SC-17 (3) (1982).

[4]   Neil H.E. Weste, David Harris, Principles of CMOS VLSI Design: A System Perspective, (3rd ed.) Addison-Wesley (2004).

[5]   Tyler Thorp, Dean Liu, Pradeep Trivedi, Analysis of blocking dynamic circuits, IEEE Transactions on VLSI Systems (2003), pp. 744-749.

[6]   F. Mendoza-Hernandez, M. Linares-Aranda, V. Champac,Noise tolerance improvement in dynamic CMOS logic circuits, Proceedings of the lEE Circuits, Devices and Systems, vol. 153 (2006), pp. 565-573 No. 6, Dec.

[7]   Y. Ji-Ren, I. Karlsson, C. Svensson ,A true single-phase-clock dynamic CMOS circuit technique, lEEE Journal of Solid-State Circuits, 22 (Oct.)

[8]   Fang Tang, Amine Bermark,Zhouye Gu, "Low power dynamic logic design using a pseudo dynamic buffer, INTEGRATION" ,the vlsi journal 45(2012) 395-404.

[9]   A.k. Pandey, R.A. Mishra, R.K. Nagaria,Low power dynamic buffer circuit, VLSICS, VoI.3,No.5,Oct.20 12,Pg.53-65.

[10]   V. Kursun, E. G. Friedman, Domino logic with variable threshold voltage keeper, IEEE Transactions on VLSI Systems, 11 (6) (2003), pp. 1080-1093.

[11]   Jan M. Rabey, Anantha Chandrakasan, Borivoje Nikolic, Digital Integrated Circuits- A Design Perspective,(2nd ed.) Prentice Hall (2003).